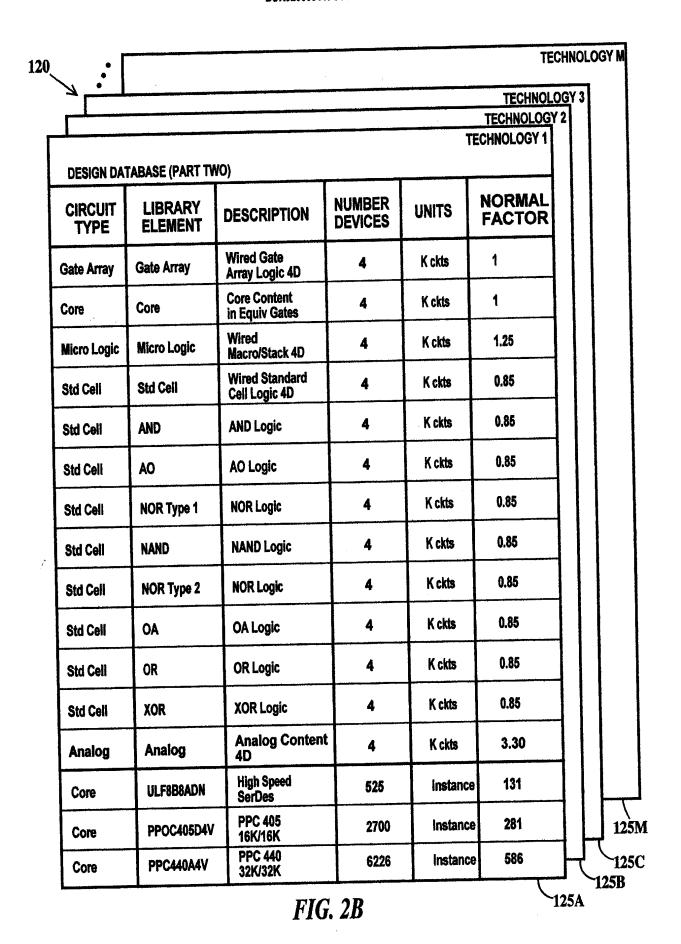


FIG. 1

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ALL DESIGN	NELEMENT FILE (P	ART ONE)		1 61	JINOLOGI I	
CIRCUIT TYPE	LIBRARY ELEMENT	DESCRIPTION	NUMBER DEVICES	UNITS	NORMAL FACTOR	
ROS	ROS	ROM 1D	1	K bits	0.05	
DRAM	Fixable DRAM	DRAM Macro 1D	1	K bits	0.11xRf	
PLA	PLA	PLAS counted as two ROMs	2	K bits	0.11	
Fixable SRAM	SRAM	1 Port Eq 6D SRAM	4	K bits	0.42xRf	
SRAM	SRAM	1 Port Eq 6D SRAM	6	K bits	0.42	
SRAM	SRAM1A	1 Port SRAM Compileable	6	K bits	0.42	
SRAM	SRAM1P	1 Port SRAM Compileable	6	K bits	0.42	
SRAM	SRAM1R	1 Port SRAM w/Redundancy	6	K bits	0.42	
SRAM	SRAM1LG	1 Port SRAM Low Power	6	K bits	0.42	
SRAM	SRAM1G	1 Port SRAM Compileable	6	K bits	0.42	
SRAM8	SRAM2G	2 Port SRAM Compileable	8	K bits	0.56	
Register	Register	Register array Bits & Latches	10	K bits	0.85	
TCAM	SRAM	IP Cores in Equiv Gate Array	16	K bits	1.27	
OCD	OCD	Off Chip Driver Circuits	30	K counts	6.76	
IOS	IOS	Input/Output Ckts Rcvr&OCD (n+m)D	40	K counts	9.05	125B

FIG. 2A

125A



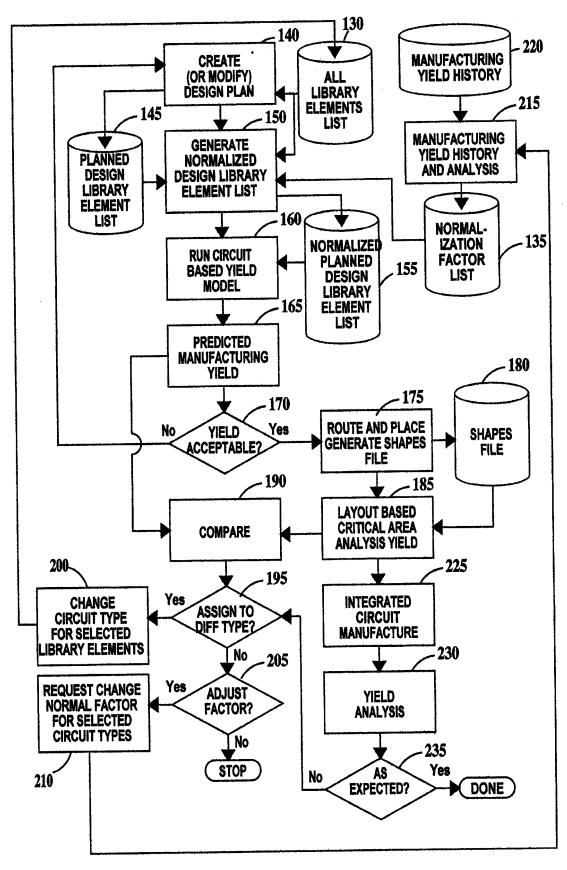


FIG. 3

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NORMALIZED PLANNED DESIGN LIBRARY ELEMENT LIST								
LIBRARY ELEMENT	CIRCUIT COUNT	CIRCUIT TYPE	NORMALIZATION FACTOR	EQUIVALENT CIRCUIT COUNT				
EA1	1000	TA	.5	500				
EA2	1000	TA	.5	500				
EB1	500	ТВ	.75	375				
EB3	200	ТВ	.75	150				
EB10	100	ТВ	.75	75				
EC2	10	TC	2.5	25				
EC3	20	тс	2.5	50				
ED1	200	TD	.5	100				
ED4	150	TD	.5	75				
TOTAL	4950			1850				

*FIG.* 4

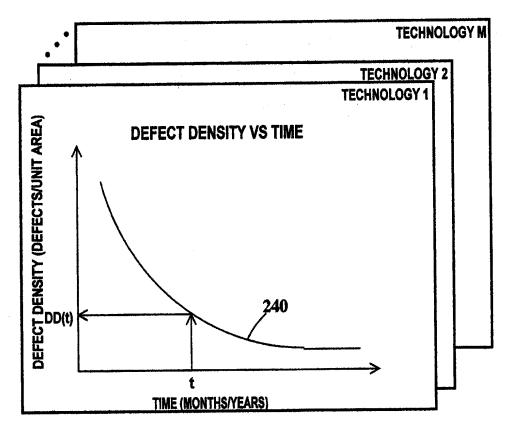


FIG. 5

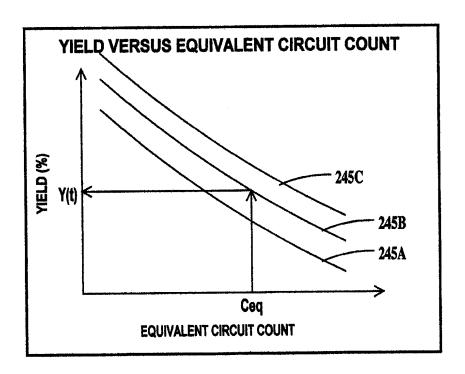


FIG. 6

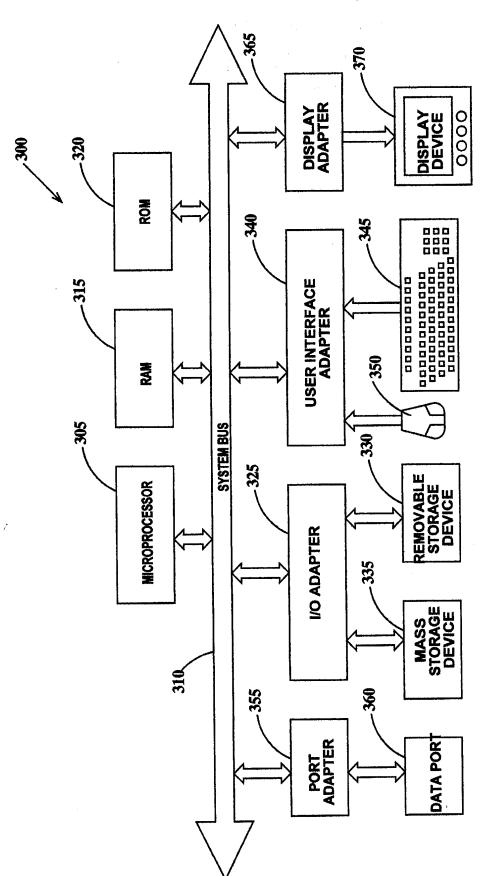


FIG. 7